What is claimed is:

1. A method for forming a gate electrode for a multiple gate transistor in a semiconductor device, comprising:

providing a substructure comprising a semiconductor fin disposed over an insulating layer and a gate dielectric formed on said semiconductor fin;

forming a gate electrode material over said gate dielectric and said semiconductor fin, said gate electrode material having a top surface that is non-planar as formed;

introducing dopant impurities into said gate electrode material;

after said introducing, annealing to activate said dopant impurities in said gate electrode material; and

planarizing said top surface to form a planarized top surface.

2. The method as in claim 1, wherein said planarizing follows said introducing and said annealing.

3. The method as in claim 1, wherein said planarizing precedes said introducing and said annealing.

4. The method as in claim 3, wherein said gate dielectric includes nitrogen therein.

5. The method as in claim 1, further comprising patterning said gate electrode material to produce a gate electrode that traverses said semiconductor fin and includes said planarized top surface.

6. The method as in claim 5, further comprising forming source and drain regions in said semiconductor fin adjacent each of opposed sides of said gate electrode.

7. The method as in claim 6, further comprising forming spacers on sides of said gate electrode and forming a silicide in at least one of said gate electrode and said source and drain regions.

8. The method as in claim 5, further comprising:
forming spacers on sides of said gate electrode;
performing selective epitaxy on exposed portions of said semiconductor fin; and
forming source and drain regions in said semiconductor fin adjacent each of opposed sides of said gate electrode.

9. The method as in claim 5, wherein said patterning comprises forming a patterned masking layer over said gate electrode material and etching portions of said gate electrode material not covered by said patterned masking layer.

10. The method as in claim 9, wherein said etching comprises plasma etching.

11. The method as in claim 9, further comprising introducing dopant impurities into said semiconductor fin to form source and drain regions therein prior to removing said patterned masking layer.

12. The method as in claim 1, wherein said forming a gate electrode material comprises forming a substantially conformal film.

13. The method as in claim 1, wherein said semiconductor fin is formed of silicon.

14. The method as in claim 1, wherein said semiconductor fin is formed of at least silicon and germanium.

15. The method as in claim 1, wherein said semiconductor fin is a lead extending longitudinally over said insulating layer and having a height greater than its width.

16. The method as in claim 1, wherein said introducing comprises introducing one of P-type dopant impurities, said P-type dopant impurities including at least one of boron and indium, and N-type dopant impurities, said N-type dopant impurities including at least one of phosphorus, arsenic, and antimony.

17. The method as in claim 1, wherein said introducing comprises one of ion implantation and plasma immersion ion implantation and includes a dopant impurity dose of at least $1x10^{15}$ cm^{-2}.

18. The method as in claim 1, wherein said providing includes said substructure including a masking layer formed over a top surface of said semiconductor fin and said forming further includes forming said gate electrode material over said masking layer.

19. The method as in claim 1, wherein said gate dielectric covers sidewalls and a top of said semiconductor fin.

20. The method as in claim 1, wherein said providing includes said insulating layer having a depressed portion encroaching said semiconductor fin and resulting in a notch, and wherein said forming a gate electrode material includes filling said notch.

21. The method as in claim 1, wherein said gate dielectric is formed of one of silicon oxide and of silicon oxynitride.

22. The method as in claim 1, wherein said gate dielectric includes at least one of La_2O_3, Al_2O_3, HfO_2, HfON, and ZrO_2.

23. The method as in claim 1, wherein said gate dielectric is formed of a material having a permittivity, relative to free space, being greater than 5.

24. The method as in claim 1, wherein said gate electrode material comprises polycrystalline silicon.

25. The method as in claim 1, wherein said gate electrode material is formed of a conductive material.

26. The method as in claim 1, wherein said planarizing produces said gate electrode material having a height substantially greater than a semiconductor fin height.

27. A method for forming a gate electrode for a multiple gate transistor in a semiconductor device, comprising:

providing a substructure comprising a semiconductor fin disposed over an insulating layer and a gate dielectric disposed on said semiconductor fin;

forming a gate electrode material over said gate dielectric and said semiconductor fin, said gate electrode material having a top surface that is non-planar as formed;

introducing dopant impurities into said gate electrode material;

after said introducing, annealing to activate said dopant impurities within said gate electrode material; and

after said annealing, planarizing said top surface to form a planarized top surface.

28. A method for forming a gate electrode for a multiple gate transistor in a semiconductor device, comprising:

providing a substructure comprising a semiconductor fin disposed over an insulating layer and a gate dielectric disposed on said semiconductor fin;

forming a gate electrode material over said gate dielectric and said semiconductor fin, said gate electrode material having a substantially planar top surface;

after said forming, introducing dopant impurities into said gate electrode material; and

after said introducing, annealing to activate said dopant impurities within said gate electrode material.

29. The method as in claim 28, wherein said forming a layer of said gate electrode material comprises forming a layer of said gate electrode material having a top surface that is non-planar as formed, then planarizing said top surface to produce said gate electrode material having a substantially planar top surface.

30. A method for forming a gate electrode for a multiple gate transistor in a semiconductor device, comprising;

providing a substructure comprising a semiconductor fin disposed over an insulating layer and a gate dielectric disposed on said semiconductor fin, said semiconductor fin being a lead extending longitudinally over said insulating layer and having a height greater than its width;

forming a gate electrode material over said gate dielectric and said semiconductor fin, said gate electrode material having a non-planar top surface;

introducing dopant impurities into said gate electrode material;

after said introducing, annealing to activate said dopant impurities in said gate electrode material;

planarizing said top surface to form a planarized top surface;

forming a patterned masking layer over said gate electrode material;

etching portions of said gate electrode material not covered by said patterned masking layer to produce a gate electrode that traverses said semiconductor fin;

with said patterned masking layer in place, introducing dopant impurities into said semiconductor fin to form source and drain active regions therein; and

then removing said patterned masking layer.

31. The method as in claim 30, further comprising forming spacers on sidewalls of said gate electrode and epitaxially growing a further film on exposed portions of said source and drain active regions.